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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
YANCHUS III, PAUL B	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 11/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/938,206	RADJASSAMY, RAJAKRISHNAN	
	Examiner	Art Unit	
	Paul B Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-36* is/are allowed.

6)☒ Claim(s) *1 and 2* is/are rejected.

7)☒ Claim(s) *3-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/16/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 26 is objected to because of the following informalities:

There is a typographical error in line 20 of claim 26. It appears that "first latch" was inadvertently omitted from line 20, in between "said" and ";". Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Rogers, US Patent no. 5,548,620.

Rogers discloses a method of transferring data from circuitry disposed in a first frequency clock domain to circuitry disposed in a second frequency clock domain, said first frequency clock domain operating with a first clock signal [SLOW] and said second frequency clock domain operating with a second clock signal [FAST], comprising the steps:

latching said data in a first latch [element 214 in Figure 2] to generate a first latched data output, said first latch operating in response to a first modified clock signal [SLOW_R] that is synthesized at least in part from said first clock signal [column 4, lines 56-65];

providing said first latched data output to a second latch [element 222 in Figure 2] disposed in said second frequency clock domain, wherein said second latch is gated by a second modified clock signal [FAST_R] synthesized at least in part from said second clock signal, said second latch operating to generate a second latched data output [column 4, lines 35-43 and Figure 3]; and

providing said second latched data output to a register [element 224 in Figure 2] clocked by said second clock signal [FAST] for generating a synchronized data output [DATA OUT in Figure 2] operable to be supplied to said circuitry disposed in said second frequency clock domain [column 5, lines 8-18].

Rogers discloses a method for transferring data from a first, slower, clock frequency domain to a second, higher, clock frequency domain. Rogers also states that the same technique can be applied to transfer data from a first, higher, clock frequency domain to a second, lower, clock frequency domain [column 5, lines 34-43]. Therefore, Rogers discloses using the method described above, to transfer data from a higher frequency clock domain to a lower frequency clock domain.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rogers, US Patent no. 5,548,620, in view of, Rozario et al., US Patent no. 6,345,328 [Rozario].

Rogers discloses a method of transferring data from a first, higher, clock frequency domain to a second, lower clock frequency domain, but does not specifically state that the first and second clock signals are provided at a ratio of [N:M], where N equals the number of cycles of said first clock signal and M equals the number of cycles of said second clock signal and further equals (N-1). However, Rozario discloses that it is well known in the art to transfer data from a conventional core clock frequency domain [CCLK at 133 MHz] to a conventional peripheral clock frequency domain [PCLK at 66MHz, column 5, lines 35-51 and column 6, lines 16-18]. The ratio between the conventional CCLK and PCLK domains is [2:1].

Allowable Subject Matter

Claims 3-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 19-36 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 19-25, the prior art of record does not explicitly teach a method for transferring data across a clock domain boundary, the method comprising latching data provided by circuitry disposed in a first clock frequency domain to generate latched data which is gated by a first modified clock signal that is based on three intermediary clock signals derived from a first clock signal, providing the latched data to a second latch that is gated by a second modified clock

signal that is synthesized based on a second clock signal and at least one intermediary clock signal derived from the second clock signal and providing the data from the second latch to a first register clocked by the second clock signal.

Regarding claims 26-36, the prior art of record does not teach a system for transferring data from circuitry operating with a first clock signal in a first clock domain to circuitry operating with a second clock signal in a second clock domain, the system comprising a latch that is gated by a first modified clock signal based on the first clock signal and a plurality of intermediary clock signals derived from the first clock signal, a second latch that is clocked by a second modified clock signal based on the second clock signal and at least one intermediary clock signal derived from the second clock signal, and a register that is clocked by the second clock signal. The first latch provides data to the second latch and the second latch provides data to the register.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Flood et al., US Patent no. 6,163,545, discloses transferring data between clock domains with frequencies that are within an integer ratio.

Lovelace et al, US Patent no. 5,930,311, discloses transferring data from a first clock domain to a second clock domain.

Nguyen, US Patent no. 5,905,766, discloses transferring data from a write clock domain to a read clock domain using registers that are clocked using modified versions of the write and read clocks.

Matsumoto, US Patent no. 5,369,672, discloses transferring data from an external clock domain to an internal clock domain.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus
November 10, 2004

THUAN DU